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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,406	12/04/2003	Torsten Partsch	2003P52602US/I331.103.101	8907

7590 02/24/2005

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EXAMINER	
AUDUONG, GENE NGHIA	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/727,406	PARTSCH ET AL.	
	Examiner	Art Unit	
	Gene N. Auduong	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-35 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-35 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 12-04-03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on December 4, 2003 is being considered by the examiner.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-35 are rejected under 35 U.S.C. 102(b) as being anticipated by Ooishi (U.S. Pat. No. 6,134,179).

Regarding claim 1, Ooishi discloses a random access memory (figure 13) comprising: a plurality of data pads (figure 13, data bus 626, 628); an array of memory cells comprising a first portion of memory cells (odd portion of memory cells) and a second portion of memory cells (even portion of memory cells); a first line configured to receive first data signals between the first portion of memory cells and the data pads (line from odd portion of memory cells configured to receive first data signals between the odd portion of memory cells and the data bus 626); and a second line configured to receive second data signals between the second portion of memory cells and the data pads (line from even portion of memory cells configured to receive second data signals between the even portion of memory cells and the data bus 628), wherein the first portion of memory cells is configured to be made inaccessible to eliminate the first data signals and a first number of the data pads and the second portion of memory cells is configured

to be made inaccessible to eliminate the second data signals and a second number of the data pads (the odd portion of memory cells is configured to be made inaccessible (not select) to eliminate the odd data signals and a first number of the data bus 626, and the even portion of memory cells is configured to be made inaccessible to eliminate the even data signals and a second number of the data bus 628; col. 14, lines 16+).

Regarding claim 2, Ooishi discloses the random access memory of claim 1, wherein the first number of the data pads is equal to the second number of the data pads (odd portion of data pads and even portion of data pads is equal to each other).

Regarding claim 3, Ooishi discloses the random access memory of claim 1, wherein the first portion (odd portion) of memory cells is separate from the second portion (even portion) of memory cells (figures 12 and 13).

Regarding claim 4, Ooishi discloses the random access memory of claim 1, wherein the first portion (odd portion) of memory cells and the second portion (even portion) of memory cells have the same number of accessible memory cells (figures 12-13).

Regarding claim 5, Ooishi discloses the random access memory of claim 1, wherein the first line comprises a first data bus that receives eight first data signals and the second line comprises a second data bus that receives eight second data signals (figure 7, 8k BL).

Regarding claim 6, Ooishi discloses the random access memory of claim 1, further comprising: word lines extending along rows of the array of memory cells (col. 6, lines 18-20); and bit lines extending along columns of the array of memory cells, wherein a memory cell is located at each cross point of one of the word lines and one of the bit lines (col. 6, lines 20+).

Regarding claim 7, Ooishi discloses the random access memory of claim 6, wherein a first portion of the bit lines is electrically coupled to the first line and a second portion of the bit lines is electrically coupled to the second line (odd portion memory cells and even portion memory cells are electrically coupled to the odd and even data line).

Regarding claim 8, Ooishi discloses the random access memory of claim 1, wherein the first portion (odd portion) of memory cells stores even data and odd data and the second portion of memory cells stores even data and odd data.

Regarding claims 8-10, Ooishi discloses the random access memory of claim 1, wherein the memory has a page length of 8k bit or 16k bits (figure 7, 16k bit page length from DQ0 to DQ15; figure 7, 16k word line; or 8k bit length).

Regarding claim 11, Ooishi discloses the random access memory of claim 1, wherein the first line comprises a fuse to be blown to deactivate the first portion of memory cells and the second line comprises a fuse to be blown to deactivate the second portion of memory cells (figure 50; col. 38, lines 1+).

Regarding claim 12, Ooishi discloses the random access memory of claim 1, comprising a multiplexer configured to select the first data signals and the second data signals and provide the selected signals to the data pads (figure 13, multiplexer 632; col. 14, lines 15+).

Claims 13-17, 18-22, 29-32 and 33-35 contain the similar limitation as previously discussed in claims 1-12. Therefore, they are analyzed as previously discussed with respect to claims 1-12.

Regarding claims 23-28, the apparatus as previously discussed in claims 1-12, 13-17, 18-22, 29-32 and 33-35 would be performed the method as claimed. Therefore, they are analyzed as previously discussed with respect to apparatus claims 1-12, 13-17, 18-22, 29-32 and 33-35.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gene N. Auduong whose telephone number is (571) 272-1773. The examiner can normally be reached on 9-5-4, alternate second Monday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GA
February 07, 2005

Gene N Auduong
Primary Examiner
Art Unit 2827